Remarks

Reconsideration of this application is requested. By this response claims 1, 6, 7, 10 and 16 have been amended and claim 3 has been canceled. Claims 1-2 and 4-20 remain in the application.

Specification - Objection to the title

The title was objected to for not being descriptive. Please change the title that occurs in the specification on page 1 and in the abstract on page 11, line 1 in both instances, to read "DYNAMICALLY CHANGING INSTRUCTION CACHE LINES MIXED WITH TRACE CACHE LINES".

Response to the 35 U.S.C. §102(e) Rejection

Claims 1-5

The Office Action rejected claims 1-20 under 35 U.S.C. §102(e) as being anticipated by Hironaka et al. (U.S. Patent Publication No. 2004/0088489).

Per this response the elements and limitations of Applicants' claim 3 were included in the amended language of claim 1. Applicants' claim 1 now recites a cache array having cache lines filled with contiguous instructions in an instruction cache (ICache) portion that is adjacent to a trace cache (TCache) portion where cache lines are filled with elements of a trace, where neither the ICache portion nor the TCache portion are looked-up when the TCache portion is supplying instructions.

The relied upon art of Hironaka et al. illustrate in FIGs. 13 and 14 that a multi-port instruction/trace integrated cache includes a plurality of banks which store instruction data. Hironakas' FIG 13 shows a tag directory that is included in claims 6-9 and described in the specification in paragraph [0137]. The tag directory 39 includes a plurality of areas each corresponding to an index set to a middle-order digit in a fetch address outputted from the parallel processor. The tag directory also includes a tag 1 and a tag 2 which specifies a top address to handle data from the trace cache, and a set 46 of trace fetch

addresses inputted as trace data from the address fill buffer 36 of the fill unit 34.

Applicants' claim 1 recites that neither the ICache portion nor the TCache portion are looked-up when the TCache portion is supplying instructions. Support for this portion of Applicants' claim 1 is found in the specification on page 5, lines 13-18, that states the TCache portion may associate a "next address" with each line that allows the next line to be ready before the current line is completely fetched. This chaining of cache lines provides an efficient implementation for semi-trace cache 20 that avoids activating a line every cycle. By holding the line-enable constant and pulling out sequential elements, the cache saves the energy normally used to index the cache.

Whereas, Hironakas' cache lines necessitate a look up operation using the tag directory that contains trace fetch addresses to index the cache, Applicants' claim 1 specifies that neither the ICache portion nor the TCache portion are looked-up when the TCache portion is supplying instructions. Accordingly, the amended language of Applicants' claim 1 is believed to have overcome the art of record and claim 1 should now be allowable.

Claims 2, 4-5 directly depend from Applicants' claim 1 and these dependent claims are also believed to be allowable for at least the same reasons as claim 1. Per this response claim 3 has been canceled and the rejection of Applicants' claim 3 is now moot.

Claims 6-9

Applicants' claim 6 recites, among other things, a cache having in one array both an instruction cache (ICache) portion and a trace cache (TCache) portion, where a line in the TCache portion is not looked-up when the TCache portion is supplying instructions.

Again, Hironakas' cache lines use the tag directory, and specifically the trace fetch addresses, to provide a lookup operation that indexes the cache. However, Applicants' claim 6 specifies that a line in the TCache portion is not looked-up when the TCache portion is supplying instructions. Accordingly, the

amended language of Applicants' claim 6 is believed to have overcome the art of record and claim 6 should be allowable.

Claims 6-9 depend, either directly for indirectly, from Applicants' claim 6 and these dependent claims are also believed to be allowable for at least the same reasons as claim 6.

Claims 10-15

Applicants' claim 10 recites intermingling cache lines in one array of a cache where a first cache line in a trace cache (TCache) portion is physically adjacent a second cache line in an instruction cache (ICache) portion and selecting the TCache or the ICache portion based on an address of the next instruction.

Hironaka describes in the specification in paragraph [0137] that tag directory 39 includes a valid bit indicating that the area 45 is valid and a trace bit as an identification bit to indicate that data is from the trace cache. Specifically, Hironaka then requires in paragraph [0139] that the trace cache is indicated by a tag 1 set to a high-order digit in the fetch address and a tag 2 set to a lower-order digit in the fetch address. These multiple conditions based on the tag 1, the tag 2 and the identification bit must be satisfied for the trace cache hit judgment circuit 48 to judge that the instruction data string to be accessed is stored in the multi-port bank memory.

Applicants claim that the TCache or the ICache portion is selected based on an address of the next instruction. Support for this language may be found in the specification on page 4, lines 12-17, that states instructions may be fetched from the TCache portion of semi-trace cache 20 with only one address/access. Again on page 5, lines 23-24, the specification states that the address is checked as to whether it is found in the TCache by determining if a hit is indicated. Whereas Hironaka determines the trace cache hit by first verifying the identification bit, Applicant claims that the TCache is selected based on an address of the next instruction. At least this feature of Applicants' claim 10 is not found in the prior art reference, and accordingly, the Hironaka reference does not anticipate Applicants' claim 10.

Claims 11-15 directly depend from Applicants' claim 10 and these dependent claims are also believed to be allowable for at least the same reasons as claim 10.

Claims 16-20

Applicants' claim 16 recites filling an array with instruction cache (ICache) cache lines mixed with trace cache (TCache) cache lines where an allocated proportion of ICache cache lines to TCache cache lines is dynamically changing with time and neither the ICache portion nor the TCache portion are looked-up when the TCache portion is supplying instructions.

As stated before, Hironaka relies on indexing to look up stored cache data. Hironaka further indicates details of the fetch of the trace cache in multi-port bank memory 43 illustrated in FIG. 15. The multiple banks force Hironaka to look up a plurality of fetch addresses to predict a bank and determine which bank may be possibly fetched. Similar to Applicants' claims 1 and 6, claim 16 recites that neither the ICache portion nor the TCache portion are looked-up when the TCache portion is supplying instructions. Since the relied upon art does not include all of Applicants' claim features it is believed that the rejection of these claims under 35 U.S.C. §102(e) has been overcome and the rejection should be removed.

Claims 17-20 depend, either directly for indirectly, from Applicants' claim 16 and these dependent claims are also believed to be allowable for at least the same reasons as claim 16.

Response to the rejection of claim 1, 10 and 16 based on Wang et al.

The Office Action rejected claims 1, 10 and 16 under 35 U.S.C. §102(b) as being anticipated by Wang et al. (U.S. Patent Publication No. 2002/0144101).

Base claim 1 has been amended to recite, among other things, a cache array having cache lines filled with contiguous instructions in an instruction cache (ICache) portion that is adjacent to a trace cache (TCache) portion where cache lines are filled with elements of a trace, where neither the ICache

portion nor the TCache portion are looked-up when the TCache portion is supplying instructions.

Wang et al. teach in paragraph [0022] that the DAG trace cache 22 includes a tag array and a data array. To locate a DAG trace in trace cache 22, DAG extractor 30 uses an instruction address or instruction pointer as key to perform an associative lookup on the tag array of the trace cache. Wang et al. clearly states that a lookup is performed when the trace cache is supplying instructions, which is in contrast to Applicants' base claim 1. Accordingly, the Wang prior art reference cannot anticipate Applicants' claim 1 and the rejection of Applicants' claim under 35 U.S.C. 102(b) should be removed.

Base claim 10 has been amended to recite intermingling cache lines in one array of a cache where a first cache line in a trace cache (TCache) portion is physically adjacent a second cache line in an instruction cache (ICache) portion and selecting the TCache or the ICache portion based on an address of the next instruction.

Wang et al. teach in paragraph [0021] that "criterion instructions" or long latency instructions may be identified by hint bits and included by a compiler as candidates for DAG trace cache 22 at runtime. Alternatively, hardware may use a dynamic detection mechanism to identify "criterion instructions" at runtime. The hardware then tracks and maintains a table of candidate "criterion instructions". However, whether hint bits or a table are used to identify the "criterion instructions" as candidates for trace cache 22, Wangs' method is contrary to Applicants' claimed method of selecting the TCache or the ICache portion based on an address of the next instruction. Neither hint bits nor a table are equivalent to an address, and therefore, Wang et al. does not anticipate Applicants' claim 10.

Base claim 16 has been amended to recite filling an array with instruction cache (ICache) cache lines mixed with trace cache (TCache) cache lines where an allocated proportion of ICache cache lines to TCache cache lines is dynamically changing with time and neither the ICache portion nor the TCache portion are looked-up when the TCache portion is supplying instructions.

As previously mentioned, Wang et al. teach in paragraph [0022] that a lookup is performed when the trace cache is supplying instructions, which is contrary to the claim language of Applicants' base claim 16. Accordingly, the Wang prior art reference cannot anticipate Applicants' claim 16 and the rejection of Applicants' claim under 35 U.S.C. 102(b) should be removed.

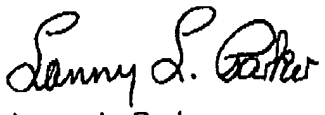
Conclusion

The foregoing is submitted as a full and complete response to the Office Action. Reconsideration of the rejections is requested. It is submitted that claims 1, 2 and 4-20 are now in condition for allowance. Allowance of these claims is earnestly solicited.

Applicants herewith petition the Director of the United States Patent and Trademark Office to extend the time for response to the Office Action dated February 27, 2006, for 1 month. Please charge Deposit Account #50-0221 in the amount of $120.00 for a one month extension. Should it be determined that an additional fee is due under 37 CFR §1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #50-0221.

If the Examiner believes that there are any informalities that can be corrected by an Examiner's amendment, a telephone call to the undersigned at (480) 715-5388 is respectfully solicited.

Respectfully submitted,
Mike W. Morrow



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